QP CODE: 18103826

18103826

Reg No : .....

Name : .....

B.Sc.DEGREE(CBCS)EXAMINATION, DECEMBER 2018

First Semester

B.Sc Computer Science Model III

Complementary Course - EL1CMT06 - ELECTRONICS - FUNDAMENTALS OF DIGITAL SYSTEM

2018 Admission only

46142D55

Maximum Marks: 80 **Time: 3 H**

Part A

Answer any **ten** questions.

Each question carries **2** marks.

1. (a) Determine the value of each digit in 939. (b) How high can you count with 4 bits?
2. Conver the decimal pairs -46 and 25 to binary and add using the 2's complement form.
3. State the rules for hexadecimal addition citing suitable examples.
4. Find the binary and hexadecial equivalent of 14768.
5. Implement the truth table and the logic circuit for the expression X=A'BC+AB'C'
6. Implement the expression ABC+DE with NAND logic.
7. Determine the truth table for the following standard POS expression (A+B+C)(A+B'+C)(A+B'+C') (A'+B+C')(A'+B'+C).
8. Design a 4X1 MUX.
9. Explain the operation of a gated SR latch
10. What is meant by present and next state?
11. Why are shift register considered basic memory devices?
12. How a shift register counter differs from a basic shift register?

(10×2

Part B

Answer any **six** questions.

Each question carries **5** marks.

13. Perform the indicated operations. (a) 1101+1011 (b) 1100-1001 (c) 1110x1101 (d) 1001÷11.

14. Describe the functional differences between a NOR gate and a negative AND gate. Do they both have the same truth table?

15. Establish NOR gate as a Uiversal logic element

16. Realize the Basic gates using NAND and NOR gates.

17. Discuss commutative and associative laws of addition and multiplication in boolean algebrae.

18. Convert the expression AB'C+(AB)'+ABC'D to standard SOP form.

19. Develop a timing diagram and combinational logic circuit for the function X(=A(B+C))'

20. Compare a latch and a flip flop.

21. Design an asynchronous mod-12 counter

(6×5=30)

Part C

Answer any **two** questions.

Each question carries **15** marks.

22. Give an account of alphanumeric codes. (a) ASCII (b) EBCDIC and ©Parity Codes.

23. Using Boolean algebrae techniques simplify the following expressions and implement using logic gates of both before and after simplification (a) AB+A(B+C)+B(B+C) (b) (AB+AC)'+A'B'C (c) AB'C(BD+CDE)+AC'

24. Design a four bit magnitude comparator which checks for equality greater than and less than conditions.

25. With neat diagram and waveform explain a synchronous (a) decade counter (a) mod 12 counter

(2×15=30)

QP CODE: 19101226

19101226

Reg No : .....

Name : .....

B.Sc.DEGREE (CBCS) EXAMINATION, DECEMBER 2018

First Semester

B.Sc Computer Science Model III

Complementary Course - EL1CMT06 - ELECTRONICS - FUNDAMENTALS OF DIGITAL SYSTEMS

2017 Admission (Reappearance)

FB5EBAA1

Maximum Marks: 80 **Time: 3 Hours**

Part A

Answer any **ten** questions.

Each question carries **2** marks.

1. Convert (a) 104410 (b) 2673410 (c) 54376510 (d) 7543910 to its corresponding binary.
2. Find the 1's and 2's complement of the binary number (a) 11001011 (b) 1110001010 (c) 110000011 (d) 1111100111.
3. What is overflow condition in signed arithmetic? (b) Express +136 and -136 as an 8-bit number in the 1's complement form.
4. List the steps for converting a binary number to hexadecimal equivalent.
5. (a) When is the outpput of a NAND gate low? (b) When is th output of a NOR gate high?
6. Use NOR gates to imlement the expression (a) X=A'+B (b) X=AB.
7. Define the terms variable, complement and literal.
8. What are the peculiarities of even and odd parity checkers?
9. What are the applications of flip flops?
10. Draw the logic circuit for a master slave J-K flip flop.
11. How can shift register be used to generate a time delay?
12. What are the applications of shift registers?

(10×2=20)

Part B

Answer any **six** questions.

Each question carries **5** marks.

13. Find the Octal equivalent of the following decimal numbers (a) 54609.014 (b) 5436.31 (c) 9132 (d) 2139.64.

14. With suitable wave form, truth tables and logic symbols explain basic gates.

15. Develop a logic circuit that will produce a 1 on its output only when all three inputs are 1s or when all three inputs are 0's.

16. Implement the expression (a) X=((A'+B'+C')DE)' by using NAND logic (b) X= ((A'B'C'+(D+E))' using NOR logic.

17. State and explain De-morgans theorems.

18. Simplify the expression and implement using logic gats. (a) (AB+AC)'+A'B'C (b) A'BC+AB'C'+A'B'C'+AB'C+ABC.

19. Implement a half subtractor with suitable truth table, logic expressions and symbols.

20. List the steps/procedure for designing a synchronous counter.

21. Give an account of cascaded counters.

(6×5=30)

Part C

Answer any two questions.

Each question carries 15 marks.

22. (a) Give an account of numbering systems citing suitable examples. (b) Find the binary, octal and hexadecimal equivalent of the following decimal numbers (a) 10.75 (b) 543.075 (c) 2345.275

23. Simplify using K-Mapand draw the logic diagram after simplification (a) F(A,B,C,D)=(5,7,8,9,13,15) (b) Y=A'B'C'+A'BC'+AB'C'+ABC' (c) Y=(A'+B+C)(A+B+C')

24. With relevant figures explain a (a) priority BCD encoder (b) 8X1 MUX.

25. With neat diagram and waveform explain an asynchronous (a) mod 12 counter (d) decade counter

(2×15=30)