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(Pages : 2) Reg. No.....

Name.....

B.Sc. DEGREE (C.B.C.S.) EXAMINATION, JUNE 2018

Second Semester

Core Course—CS2 CRT 04—COMPUTER ORGANIZATION AND ARCHITECTURE

(Common to Computer Science M III, IT and B.C.A. Programmes)

[2017 Admissions only]

Time : Three Hours Maximum : 80 Marks

Part A

Answer any **ten** *questions.*
Each question carries 2 *marks.*

1. What is the significance of addressing mode ? Explain any one addressing mode.
2. Explain different instruction code formats.
3. What is hit ratio ?
4. Explain the fetch cycle.
5. What is a status register ? Explain the status bits.
6. What is a super computer ?
7. Define interrupt. List the types of interrupts.
8. What is control word ?
9. What is SISD ?
10. What is an accumulator ?
11. Explain multiprocessing system.
12. What is a One-Address instruction ? List any two One-Address instructions.

(10 × 2 = 20 marks)

Part B

Answer any **six** *questions.*
Each question carries 5 *marks.*

13. Explain different instruction code formats.
14. Explain how the reverse polish notation is suitable for stack manipulation.
15. With the help of a diagram explain Set-Associative Mapping.

Turn over

16. What are data transfer instructions ? List the data transfer instructions.

17. Explain microprogrammed Control Unit.

18. Explain vector processing.

19. Explain the memory hierarchy in a Computer system.

20. What is an array processor ? Explain SIMD array processor.

21. Give an account of Virtual Memory.

(6 × 5 = 30 marks)

Part C

Answer any two *questions.*
Each question carries 15 *marks.*

22. Describe the instruction cycle in detail.

23. Explain the stack organization in CPU.

24. What is pipelining ? Explain arithmetic, instruction and RISC pipeline.

25. Explain the various addressing modes with the help of example.

(2 × 15 = 30 marks)